



# High Speed CMOS Logic – 54HC04

## Hex Inverter Gate Logic IC in bare die form

Rev 1.0  
22/04/19

### Description

The 54HC04 hex inverter gate is fabricated on a 2.5µm CMOS process combining high speed LSTTL performance with CMOS low power. The device contains six independent inverters with standard push-pull outputs which perform the Boolean function  $Y = \bar{A}$  in positive logic. Internal circuitry comprises of three stages and includes buffered output for high noise immunity and stability. Inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

### Features:

- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- Function compatible with 54LS04
- High Noise Immunity CMOS process
- Full Military Temperature Range.

### Ordering Information

The following part suffixes apply:

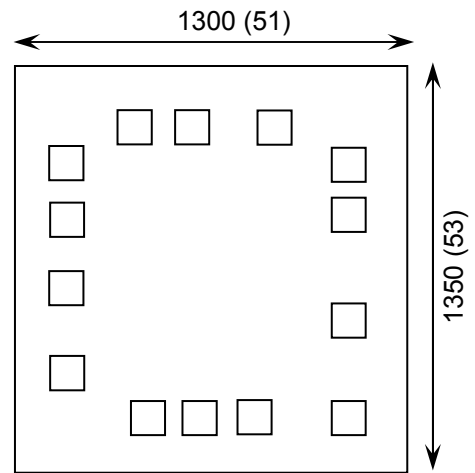
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "H" - MIL-STD-883 /2010B Visual Inspection  
+ MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-883 /2010A Visual Inspection (Space)  
+ MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

[www.siliconsupplies.com/quality/bare-die-lot-qualification](http://www.siliconsupplies.com/quality/bare-die-lot-qualification)

### Die Dimensions in µm (mils)



### Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

### Mechanical Specification

Die Size (Unsawn)	1300 x 1350 51 x 53	µm mils
Minimum Bond Pad Size	106 x 106 4.17 x 4.17	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

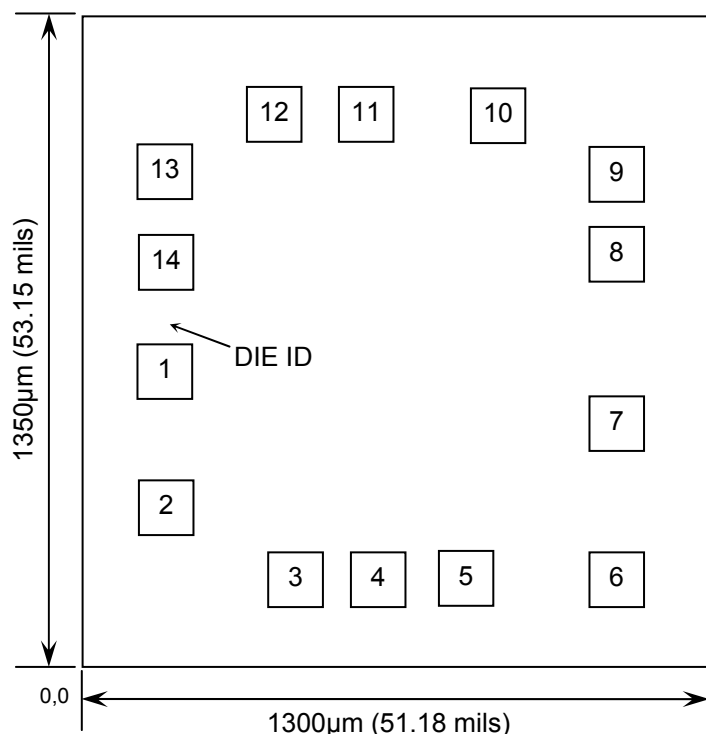




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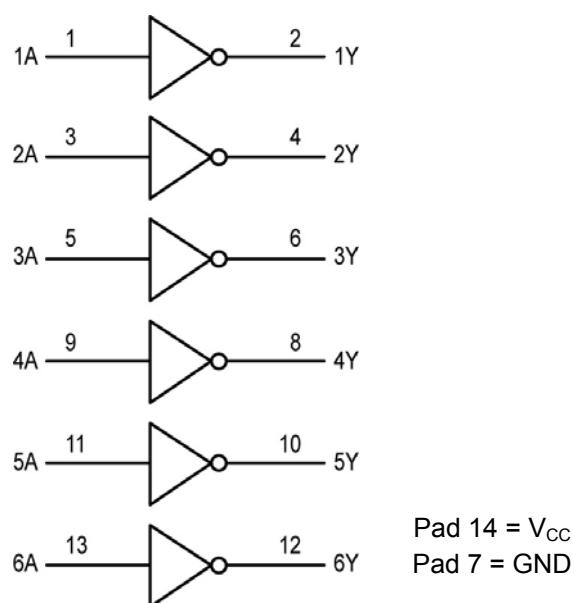
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## Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	1A	0.112	0.555
2	1Y	0.112	0.2705
3	2A	0.3815	0.12
4	2Y	0.5535	0.12
5	3A	0.7365	0.12
6	3Y	1.047	0.12
7	GND	1.047	0.4445
8	4Y	1.047	0.798
9	4A	1.047	0.967
10	5Y	0.802	1.085
11	5A	0.5295	1.085
12	6Y	0.338	1.085
13	6A	0.112	0.967
14	V <sub>CC</sub>	0.112	0.7835
CONNECT CHIP BACK TO V <sub>CC</sub> OR FLOAT			

## Logic Diagram



## Truth Table

INPUTS		OUTPUT
A		Y
H		L
L		H

H = High level (steady state)  
L = Low level (steady state)





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## Absolute Maximum Ratings<sup>1</sup>

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	$V_{CC}$	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC Output Voltage (Referenced to GND)	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
DC Input Current	$I_{IN}$	±20	mA
DC Output Current, per pad	$I_{OUT}$	±25	mA
DC Supply Current, $V_{CC}$ or GND	$I_{CC}$	±50	mA
Power Dissipation in Still Air <sup>2</sup>	$P_D$	750	mW
Storage Temperature Range	$T_{STG}$	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

## Recommended Operating Conditions<sup>3</sup> (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS	
Supply Voltage	$V_{CC}$	2	6	V	
DC Input or Output Voltage	$V_{IN}, V_{OUT}$	0	$V_{CC}$	V	
Operating Temperature Range	$T_J$	-55	+125	°C	
Input Rise or Fall Times	$t_r, t_f$	$V_{CC} = 2V$	0	1000	ns
		$V_{CC} = 4.5V$	0	500	
		$V_{CC} = 6.0V$	0	400	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	$V_{CC}$	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Minimum High-Level Input Voltage	$V_{IH}$	2.0V	$V_{OUT} = 0.1V \text{ or } V_{CC} - 0.1V$ $ I_{OUT}  \leq 20\mu A$	1.5	1.5	1.5	V
		3.0V		2.1	2.1	2.1	
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	$V_{IL}$	2.0V	$V_{OUT} = 0.1V \text{ or } V_{CC} - 0.1V$ $ I_{OUT}  \leq 20\mu A$	0.5	0.5	0.5	V
		3.0V		0.9	0.9	0.9	
		4.5V		1.35	1.35	1.35	
		6.0V		1.8	1.8	1.8	

4.  $-55^\circ C \leq T_J \leq +125^\circ C$





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## DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Minimum High-Level Output Voltage	V <sub>OH</sub>	2.0V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20μA	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		3.0V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 2.4mA	2.48	2.34	2.20	V
		4.5V		3.98	3.84	3.70	
		6.0V		5.48	5.34	5.20	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	2.0V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20μA	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		3.0V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 2.4mA	0.26	0.33	0.40	V
		4.5V		0.26	0.33	0.40	
		6.0V		0.26	0.33	0.40	
Maximum Input Leakage Current	I <sub>IN</sub>	6.0V	V <sub>IN</sub> = V <sub>CC</sub> or GND	±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Leakage Current	I <sub>CC</sub>	6.0V	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0μA	1	10	40	μA

## AC Electrical Characteristics<sup>5</sup>

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Maximum Propagation Delay, Input A or B to Output Y (Figure 1,2)	t <sub>PLH</sub> , t <sub>PHL</sub>	2.0V	C <sub>L</sub> = 50pF, t <sub>r</sub> = t <sub>f</sub> = 6ns	75	95	110	ns
		3.0V		30	40	55	
		4.5V		15	19	22	
		6.0V		13	16	19	
Maximum Output Rise and Fall Time, Any Output (Figure 1,2)	t <sub>TLH</sub> , t <sub>THL</sub>	2.0V	C <sub>L</sub> = 50pF, t <sub>r</sub> = t <sub>f</sub> = 6ns	75	95	110	ns
		3.0V		27	32	36	
		4.5V		15	19	22	
		6.0V		13	16	19	

5. Not production tested in die form, characterized by chip design and tested in package.





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## AC Electrical Characteristics Continued<sup>5</sup>

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Maximum Input Capacitance	C <sub>IN</sub>	-	-	10	10	10	pF
Power Dissipation Capacitance Per Gate <sup>6</sup>	C <sub>PD</sub>	-	T <sub>A</sub> = 25°C, V <sub>CC</sub> = 5.0V	TYPICAL			pF
				20			

6. Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

## Switching Waveform

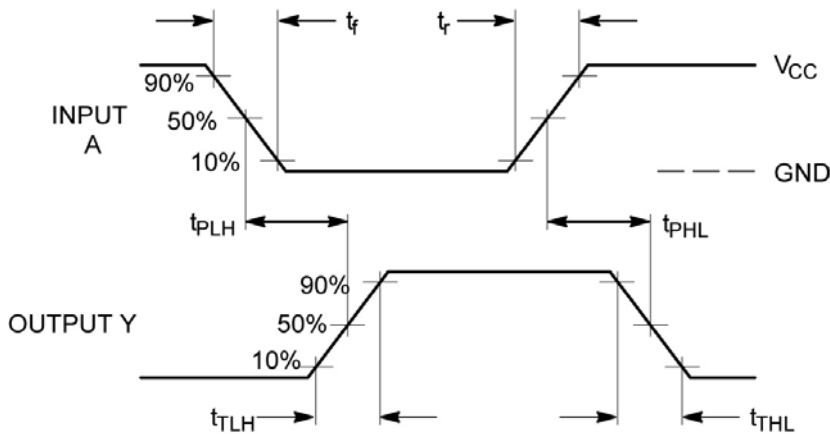
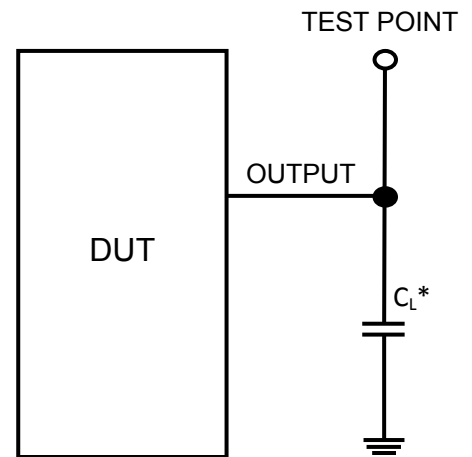


Figure 1 – Propagation Delay & Output Transition Time

## Test Circuit



\* Includes all probe and jig capacitance

Figure 2

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